

CLAIMS

- Sub 2
See Claim 1
A
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1. Shift register (21) containing a plurality of cascaded stages (J-1, J, J+1), each ^{a given stage} stage (J) being ^{responsive} connected up to two clock signals, (Q1, Q2) ^{having} containing an output (Q) and characterized in that it is connected ~~moreover~~ to the output of the preceding stage (J-1) and to the output of the next stage (J+1), and that it includes ^{the given stage comprising} a first semiconductor output device (D1) switching the associated output (Q) between high and low values of a first clock signal (Q1), this first semiconductor device (D1) being controlled by the potential of a first node (N1) connected:
- to the output of the preceding stage ~~via~~ across a second semiconductor device (D2) controlled by this same preceding output (Q),
 - to a negative potential (V-1) ~~via~~ across a third semiconductor device (D3) controlled by the output of the next stage (J+1),
 - 20 • to a second clock signal (Q2) ~~via~~ across a first capacitance (C2),
 - and to the output (Q) associated with the ^{given} stage (J) ~~via~~ across a second capacitance (C3).
2. Shift register (25) containing a plurality of cascaded stages (J-1, J, J+1), each ^{a given stage} stage (J) being ^{responsive} connected up to two clock signals (Q1, Q2) ^{having} containing an output (Q) and characterized in that it is connected ~~moreover~~ to the output of the preceding stage (J-1), and to the output of the next stage (J+1), and that it includes ^{the given stage comprising} a first semiconductor output device (D1) switching the associated output (Q) between high and low values of a first clock signal (Q1), this first semiconductor device being controlled by the potential of a first node (N1) connected:
- 35 • to the output of the preceding stage (J-1) ~~via~~ across a second semiconductor device (D2) controlled by this same preceding output (Q-1),

- to a second clock signal ~~(Φ_2)~~ ^{via} across a first capacitance ~~(C₂)~~,
 - to the output ~~(D)~~ associated with the stage ~~(J)~~ ^{assigned stage} across a second capacitance ~~(C₂)~~, the ~~said~~ output being connected to earth (33) across a third semiconductor device (T_z) controlled by a second node (Z),
 - and to earth across a fourth semiconductor device (T_d) controlled by the second node (Z),
- 10 this second node (Z) being connected moreover:
- to the output (22) of the preceding stage (J-1) across a fourth capacitance (C_c),
 - to earth across a fifth semiconductor device (T_r) controlled by the output (22) of the preceding stage
 - 15 (J-1),
 - to the output (30) of the next stage (J+1) across sixth and seventh clamping transistors (T_h, T_g) mounted in parallel and controlled, one by the second node (Z) and the other by the output (30) of the next
 - 20 stage (J+1),
 - and to that terminal of the third semiconductor device (T_z) connected to earth (33), by a capacitance (C_g).
3. Shift register (55) containing a plurality of
- 25 cascaded stages (J-1, J, J+1), each stage (J) being connected up to two clock signals (Φ_1 , Φ_2) containing an output (D) and characterized in that it is connected moreover to the output of the preceding stage (J-1) and to the output of the next stage (J+1) or of the next
- 30 but one stage (J+2), the said stage (J) including a first semiconductor output device (T_l) switching the associated selection line (J) between high and low values of a first clock signal (Φ_1), this first semiconductor device (T_l) being controlled by the
- 35 potential of a first node (G) connected:
- to the output of the preceding stage (J-1) across a second semiconductor device (T_p) controlled by this same preceding output (22),

- to a second clock signal ($\Phi 2$) across a first capacitance (C2),
 - to the output (D) associated with the stage (J) across a second capacitance (Cb), the said output (D) being connected to earth (32) across a fourth semiconductor device (Tz) controlled by a second node (Z),
 - to a negative potential (V-) across a third semiconductor device (Td) controlled by the second node (Z) which is moreover connected to the output (30) of the next stage (J+1) or of the next but one stage (J+2).
4. Shift register (21) containing a plurality of cascaded stages (J-1, J, J+1), each stage (J) being connected up to two clock signals ($\Phi 1$, $\Phi 2$) containing an output (D) and characterized in that it is connected moreover to the output of the preceding stage (J-1) and to the output of the next stage (J+1), and that it includes a first semiconductor output device (T1) switching the associated output (J) between high and low values of a first clock signal ($\Phi 1$), this first semiconductor device (T1) being controlled by the potential of a first node (G) connected:
- to the output (22) of the preceding stage (J-1) across a second semiconductor device (Tp) controlled by this same preceding output (22),
 - to a signal (V) across a third semiconductor device (Td) controlled by the output of the next stage (J+1),
 - to a second clock signal ($\Phi 2$) across a first capacitance (C2),
 - and to the output (D) associated with the stage (J) across a second capacitance (Cb), this output (D) being connected to earth across a fourth semiconductor device (Tz) controlled by a zero-reset signal.
5. Shift register (21) containing a plurality of cascaded stages (J-1, J, J+1), each stage (J) being

- connected up to two clock signals ($\Phi 1$, $\Phi 2$) containing an output (D) and characterized in that it is connected moreover to the output of the preceding stage (J-1) and to the output of the next stage (J+1), and that it includes a first semiconductor output device (T1) switching the associated output (J) between high and low values of a first clock signal ($\Phi 1$), this first semiconductor device (T1) being controlled by the potential of a first node (G) connected:
- to the output (22) of the preceding stage (J-1) across a second semiconductor device (Tp) controlled by this same preceding output (22),
 - to a constant negative potential (V-) across a third semiconductor device (Td) controlled by a clock signal (Φa) chosen from three clock signals (Φa , Φb , Φc) [lacuna] the output of the next stage (J+1),
 - to a second clock signal ($\Phi 2$) across a first capacitance (C2),
 - and to the output (D) associated with the stage (J) across a second capacitance (Cb), this output (D) being connected to earth across a fourth semiconductor device (Tz) controlled by a zero-reset signal.
6. Shift register according to ~~the preceding claim~~ *Claim 5*, characterized in that each of the clocks (Φa , Φb , Φc) consists of short pulse (T3) lagging behind the transitions of the first ($\Phi 1$) and second ($\Phi 2$) clock signals.
7. Shift register according to ~~any one of the preceding claims~~ *Claim 1*, characterized in that the first ($\Phi 1$) and second ($\Phi 2$) clock signals are complementary.
8. Shift register according to ~~any one of the preceding claims~~ *Claim 1*, characterized in that the first capacitance (C2) has a value slightly greater than the value of the stray capacitance (Cp) of the semiconductor output device (T1).
9. Shift register according to ~~any one of claims 1 to 7~~ *Claim 1*, characterized in that the first capacitance (C2)

has a value slightly less than the value of the stray capacitance (C_p) of the semiconductor output device (T_1).

5 10. Shift register according ^{to} ~~claim 8 or 9~~, characterized in that the second capacitance (C_b) has a value substantially greater to that of the stray capacitance (C_p) of the semiconductor output device (T_1).

11. Shift register according to ^{Claim 1} ~~any one of the preceding claims~~, characterized in that the semiconductor devices (T_1 , T_p , T_d , T_z , T_r , T_h) are amorphous silicon transistors.

12. Shift register according to ^{Claim 1} ~~any one of the preceding claims~~, characterized in that the outputs (D , 22, 30) of the stages ($J-1$, J , $J+1$) are lines for addressing an active matrix of a liquid crystal screen.

13. Viewing screen containing integrated peripheral control circuits made up of selection line scanners and column scanners, characterized in that at least one of these circuits includes a shift register according to ^{Claim 1} ~~any one of the preceding claims~~.

14. Viewing screen including peripheral control circuits, integrated with or external to the substrate board on which the active matrix is deposited, and 25 which are made up of scanners (D_{j-1} , D_j , D_{j+1}) for selection lines ($j-1$, j , $j+1$) and of scanners for columns ($i-1$, i , $i+1$), characterized in that it furthermore includes a supplementary conductive column (f) crossing over the selection lines ($j-1$, j , $j+1$) and 30 capacitively coupled (C_{fi}) to each of them in such a way that corresponding coupling capacitances (C_{fi}) each have a value close to the sum of the coupling capacitances (C_{ij}) between a line (j) and the columns which it crosses ($i-1$, i , $i+1$).

15. Viewing screen according to ^{Claim 14} ~~the preceding claim~~, characterized in that associated with this supplementary conductive column (f) is a supplementary conductive line (g) capacitively coupled (C_{fg}) with it

and associated with it across a comparator circuit (40), this supplementary line (g) being coupled capacitively to each of the columns (i-1, i, i+1).

16. Viewing screen according to ~~either one of~~ claims 14 ~~and 15~~, characterized in that it includes one or more shift registers according to ^{claim 1} ~~any one of claims 1 to 12~~ as well as the supplementary lines and columns according to ~~either one of claims 14 and 15~~.

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AMEND 5
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